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   ☐ development and production
   project on _____ equipment for which there are special requirements for the _____ circuits.

2. This is a ☐ Present Application ☐ Future Application (within the next year).

3. Other comments _____

   _____

4. Please have your representative ☐ Phone Me ☐ Visit Me
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MC652F
MC652G

VARIABLE THRESHOLD HIGH-NOISE-IMMUNITY R-S FLIP-FLOP

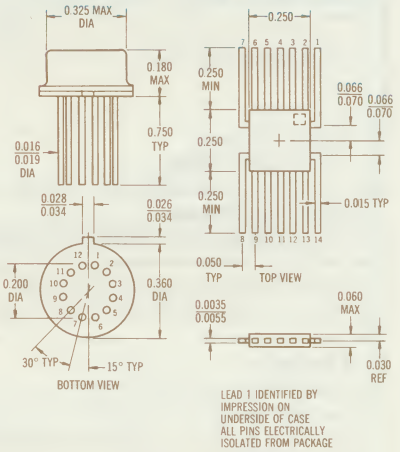
- Greater Noise Immunity than Standard Logic Circuits
- Noise Immunity Selectable from 2 volts to 5 volts
- Noise Immunity Essentially Constant over the Entire Operating Temperature Range
- Power Supply Selectable from 4 volts to 10 volts
- Two set and two reset inputs are available as individual gating circuits to allow logic operations to be performed while generating the set and reset functions.
- A shift register stage may be made by using two MC652 units.

VTL GATED R-S FLIP-FLOP INTEGRATED CIRCUIT

MONOLITHIC
SILICON EPITAXIAL PASSIVATED

AUGUST 1965 — DS 9052

12-PIN TO-5 | 14-PIN FLAT PACKAGE

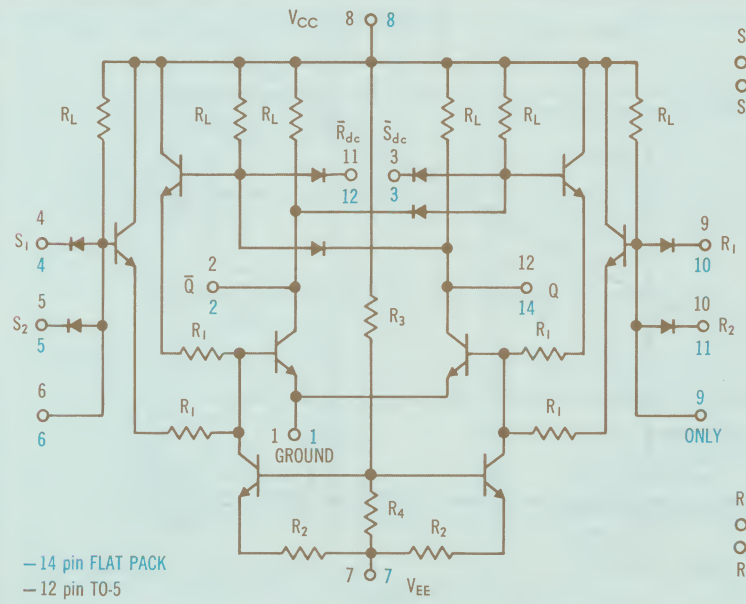


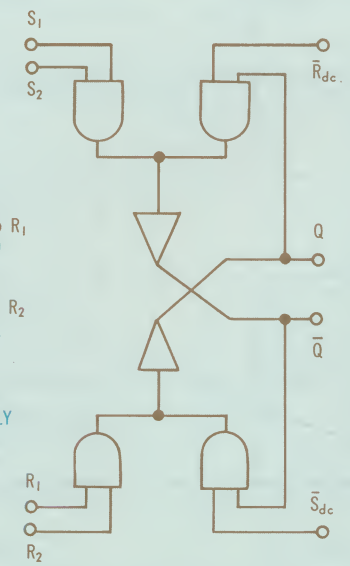
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{CC} V_{EE}	12 -12	Vdc
Input Voltage	V_{in}	12	Vdc
Current (all pins)	—	30	mAdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

NOTE: To assure correct biasing apply negative voltage to V_{EE} pin ONLY.

CIRCUIT SCHEMATIC





SET — RESET MODE*

S_1	S_2	R_1	R_2	Q^{n+1}
0	X	0	X	Q^n
0	X	X	0	Q^n
X	0	X	0	Q^n
X	0	0	X	Q^n
0	0	1	1	0
0	1	1	1	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	NA

X = don't care

DC $\overline{SET}$ — $\overline{RESET}$ MODE‡

$\overline{S}_{dc}$	$\overline{R}_{dc}$	Q^{n+1}
0	0	NA
0	1	1
1	0	0
1	1	Q^n

*$\overline{R}_{dc} = \overline{S}_{dc} = 1$
‡$(S_1 + S_2) \cdot (R_1 + R_2) = 0$

ELECTRICAL CHARACTERISTICS: V_{CC} = 10 Vdc, V_{EE} = −10 Vdc, T_A = 0 to +75°C unless otherwise noted

Characteristic	Symbol	Min	Typ	Max	Unit
Output "LOW" Voltage I_Q = 12 mA, R_1 and R_2 = V_{CC} $I_{\overline{Q}}$ = 12 mA, S_1 and S_2 = V_{CC}	Q $\overline{Q}$	— —	— —	0.725 0.725	Vdc Vdc
Output "HIGH" Voltage I_Q = -25 μA, S_1 and S_2 = V_{CC} $I_{\overline{Q}}$ = -25 μA, R_1 and R_2 = V_{CC}	Q $\overline{Q}$	9.65 9.65	— —	— —	Vdc Vdc
Input Leakage Current (V_{in} = +10 Vdc)	I_R	—	—	5.0	μAdc
Input "DOWN" Current Inputs individually to ground	I_F	—	—	3.0	mAdc
Ground DC Noise Immunity Voltage (Fan-Out = 4)	V_{NG}	—	3.7	—	Vdc
Switching Times, Figure 2 and 3 (Fan-Out = 1) Set-Reset Mode DC $\overline{Set}$-$\overline{Reset}$ Mode	 t_{d1} t_{d2} t_{d1} t_{d2}	 — — — —	 40 75 40 70	 — — — —	 nsec nsec nsec nsec
Supply Current (All Inputs Open)	I_{CC} I_{EE}	— —	— —	23.0 7.5	mAdc mAdc
Input Capacitance (f = 100 kc, Input Bias = O, unused pins grounded)	C_{in}	—	3	—	pf
Output Capacitance (f = 100 kc, Input pins grounded)	C_{out}	—	14	—	pf
Fan-Out	n	—	—	4	—

FIGURE 1 — AVERAGE POWER DISSIPATION versus POWER SUPPLY VOLTAGE

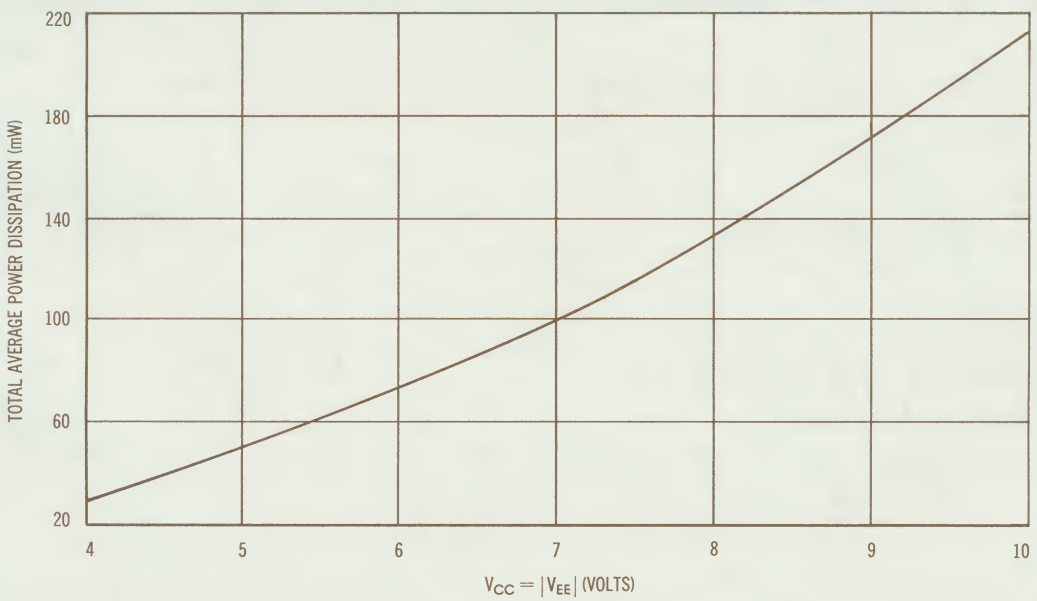


FIGURE 2 — PROPAGATION DELAY versus TEMPERATURE

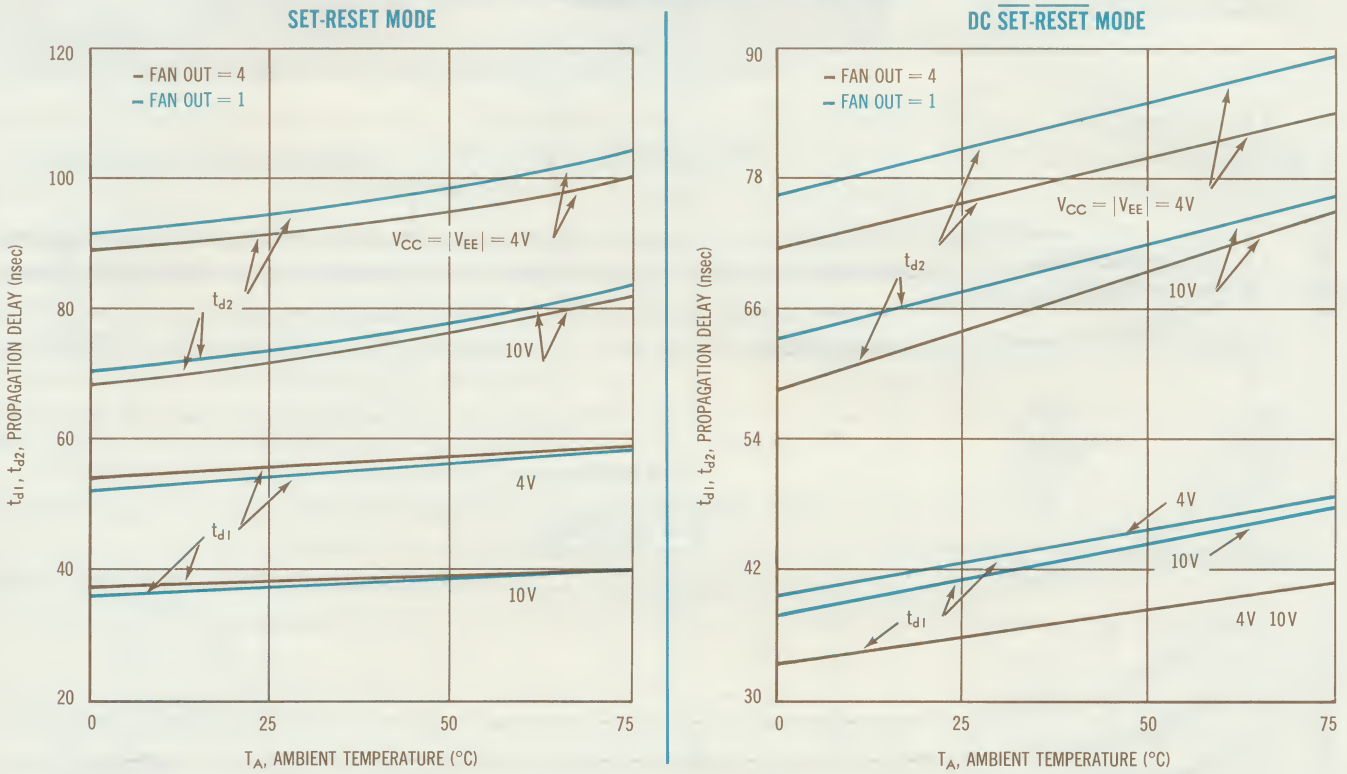
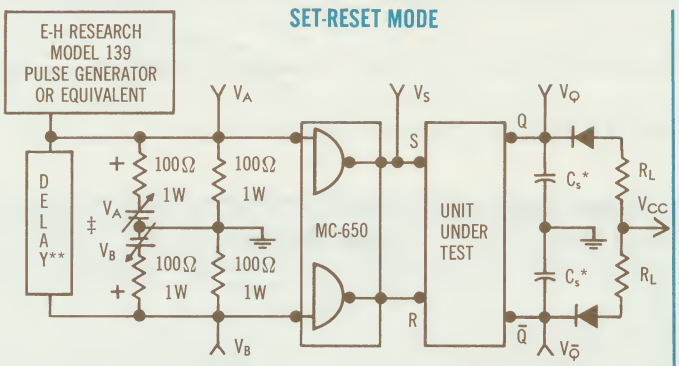
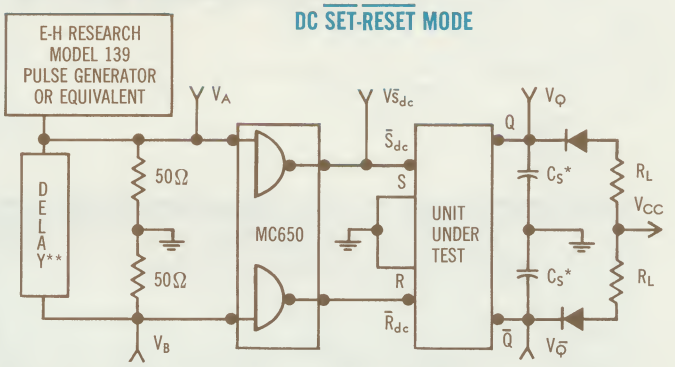


FIGURE 3 — TEST CIRCUIT PROPAGATION DELAY





$V_{CC} = |V_{EE}| = 10V$

FAN OUT	R_L ohms	C_s* pf
1	4K	4
4	1K	16

**Delay = 800 nsec, PRF ≅ 100 kc

*C_s IS TOTAL SHUNT CAPACITANCE OF TEST JIG, CONNECTORS AND ACTIVE OSCILLOSCOPE PROBE.

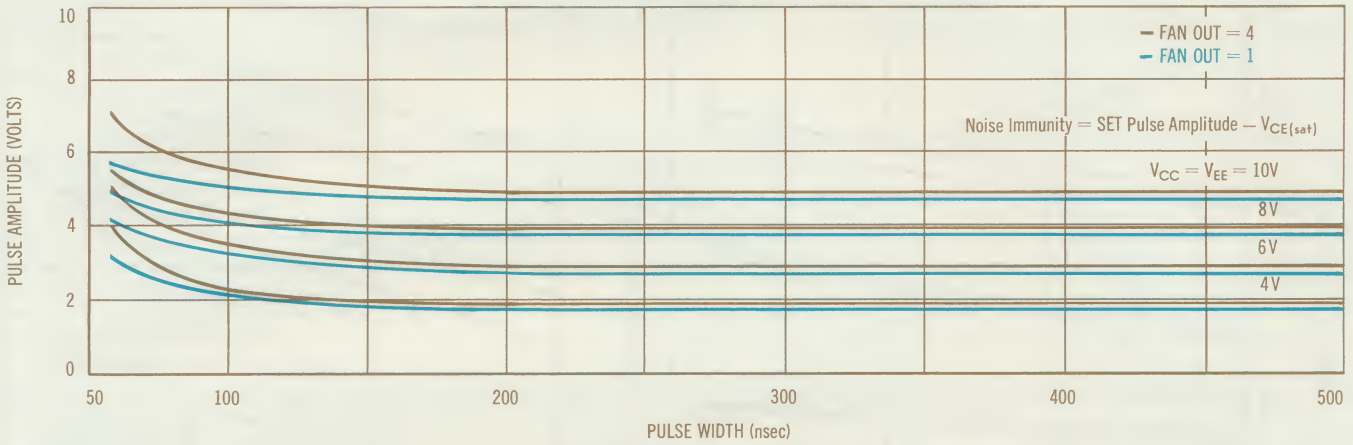
‡Adjust for DC level at points A & B to equal V_{CC}

V_B — SAME AS V_A EXCEPT DELAYED 800 nsec

V_B — SAME AS V_A EXCEPT DELAYED 800 nsec

FIGURE 4 — "SET" PULSE AMPLITUDE versus PULSE WIDTH

SET-RESET MODE



DC $\overline{\text{SET}}$-$\overline{\text{RESET}}$ MODE

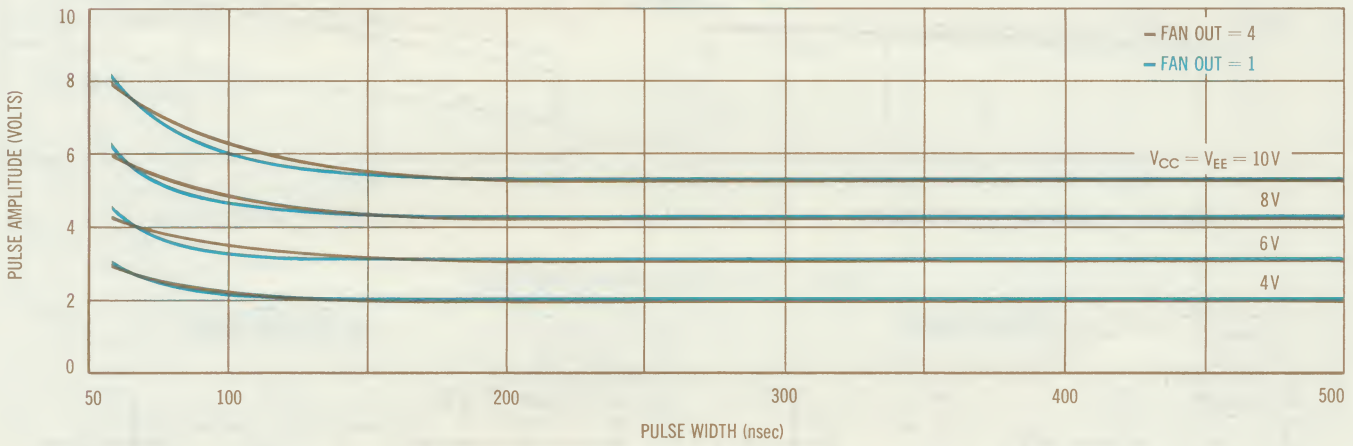
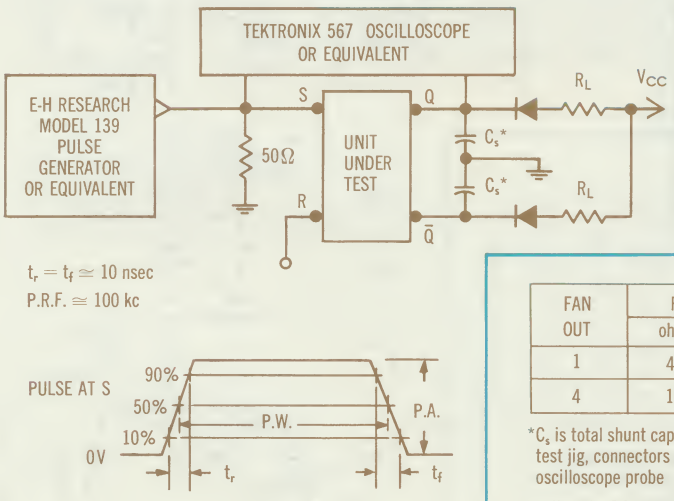


FIGURE 5 — "SET" PULSE AMPLITUDE versus PULSE WIDTH TEST CIRCUITS

SET-RESET MODE

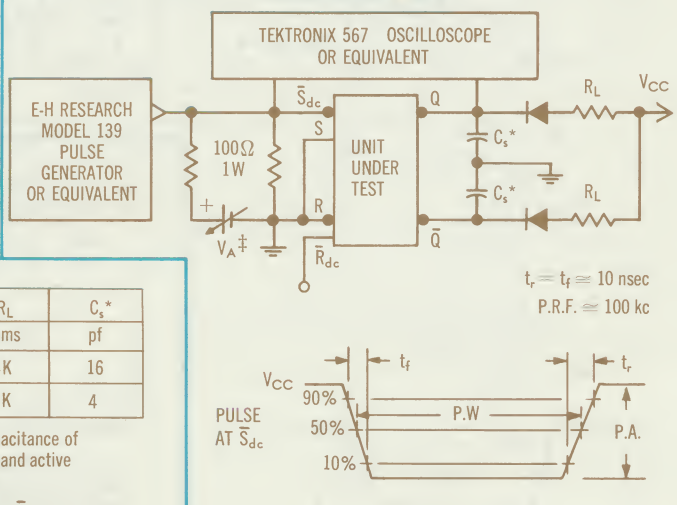


FAN OUT	R_L ohms	C_s* pf
1	4K	16
4	1K	4

*C_s is total shunt capacitance of test jig, connectors and active oscilloscope probe

‡Adjust for DC level at $\bar{S}_{dc}$ equal to V_{CC}

DC $\overline{\text{SET}}$-$\overline{\text{RESET}}$ MODE



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MC650G
DUAL 3-INPUT

MC651F
DUAL 4-INPUT

VTL NAND/NOR GATE INTEGRATED CIRCUITS

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

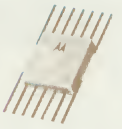
AUGUST 1965 — DS 9050

VARIABLE THRESHOLD HIGH-NOISE-IMMUNITY LOGIC GATES

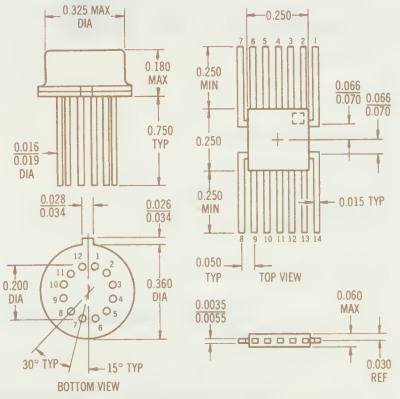
- Greater Noise Immunity than Standard Logic Circuits
- Noise Immunity Selectable from 2 Volts to 5 Volts
- Noise Immunity Essentially Constant over the Entire Temperature Range (0 to +75°C)
- Logic Swing Selectable from +4 Volts to +10 Volts
- Typical Propagation Delay 50 nsec at +25°C

12-PIN TO-5
MC650G

14-PIN FLAT PACKAGE
MC651F



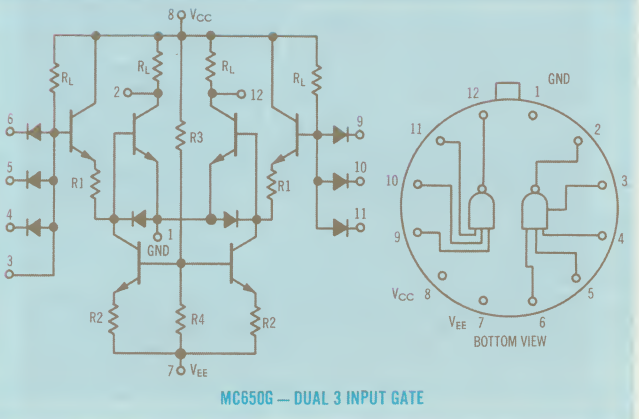
LEAD IDENTIFIED BY IMPRESSION ON UNDERSIDE OF CASE ALL PINS ELECTRICALLY ISOLATED FROM PACKAGE



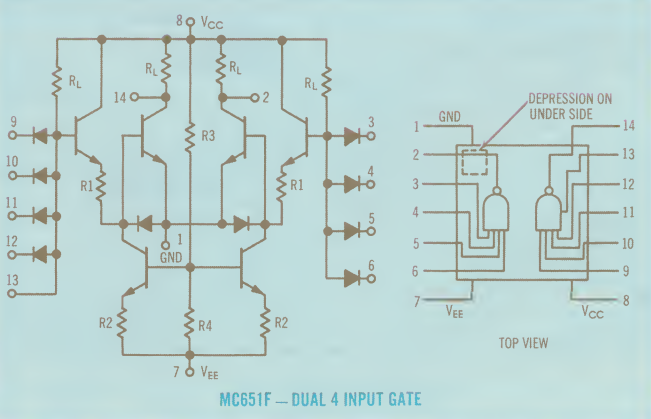
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	+12	Vdc
Power Supply Voltage	V_{EE}	-12	Vdc
Input Voltage	V_{in}	+12	Vdc
Current (All Pins)	—	30	mAdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

CIRCUIT SCHEMATIC AND LOGIC DIAGRAMS



MC650G — DUAL 3 INPUT GATE



MC651F — DUAL 4 INPUT GATE

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 Vdc, V_{EE} = −10 Vdc, T_A = 0 to +75° unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Output Saturation Voltage (I_{out} = 15 mA, All Inputs to V_{CC})		V_{max} "0"	—	—	0.725	Vdc
Output High Voltage (I_{out} = -25 μA, All Inputs to ground)		V_{min} "1"	9.65	—	—	Vdc
Input Leakage Current (V_{in} = +10 V)		I_R	—	—	5.0	μAdc
Input Down Current (Inputs individually to ground)		I_F	—	—	3.0	mAdc
TRANSFER CHARACTERISTICS	1					
Output Voltage ($V_{IL(min)}$ = 4.3 V, I_{out} = -25 μA)		V_{out}	9.55	—	—	Vdc
($V_{IH(max)}$ = 6.5 V, I_{out} = 15 mA)			—	—	0.750	
Ground DC Noise Immunity (Fan-Out = 5)	9	V_{NG}	—	3.7	—	Vdc
SWITCHING TIME	16					
Propagation Delay (Fan-Out = 5)		t_{d2}	—	45	—	nsec
Propagation Delay (Fan-Out = 1)		t_{d1}	—	55	—	nsec
Output Capacitance (f = 100 kc, input pins grounded)		C_{out}	—	11	—	pf
Input Capacitance (f = 100 kc, input bias = 0 V, unused pins grounded)		C_{in}	—	4	—	pf
Supply Current - Both Gates						
Inputs Open		I_{CC}	—	—	19	mAdc
		I_{EE}	—	—	7.5	mAdc
Inputs Ground		I_{CC}	—	—	10.0	mAdc
		I_{EE}	—	—	7.5	mAdc
Fan-Out		n	—	—	5	—

FIGURE 1 — TRANSFER CHARACTERISTIC DEFINITIONS

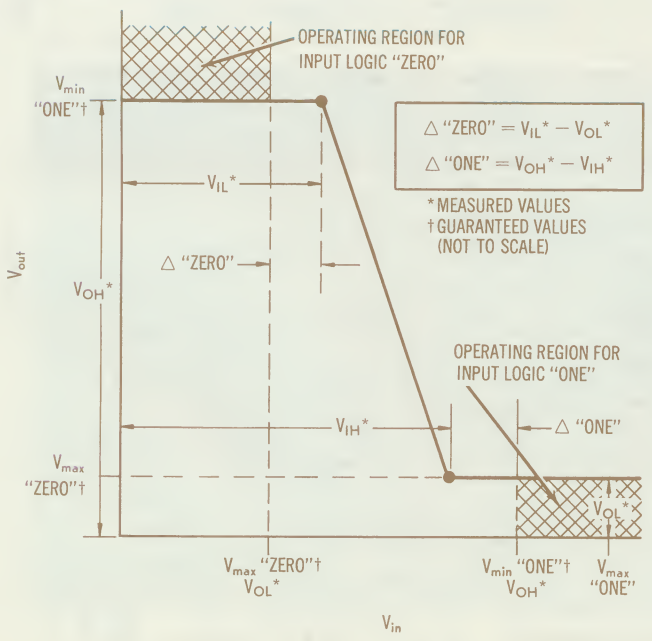
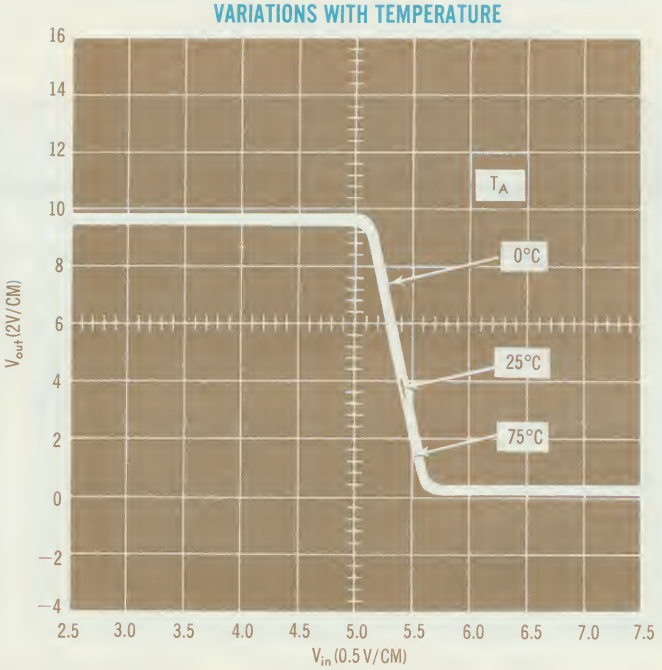
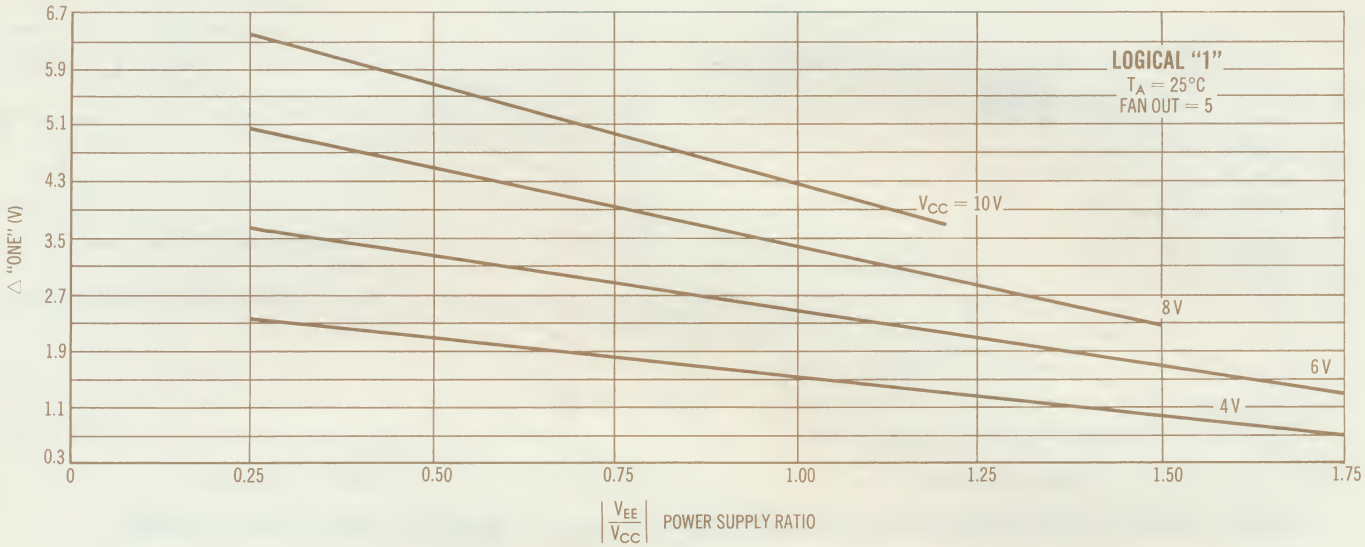


FIGURE 2 — INPUT/OUTPUT TRANSFER CHARACTERISTIC VARIATIONS WITH TEMPERATURE



TYPICAL CHARACTERISTIC CURVES

FIGURE 3 — INPUT DC NOISE MARGIN versus POWER SUPPLY RATIO



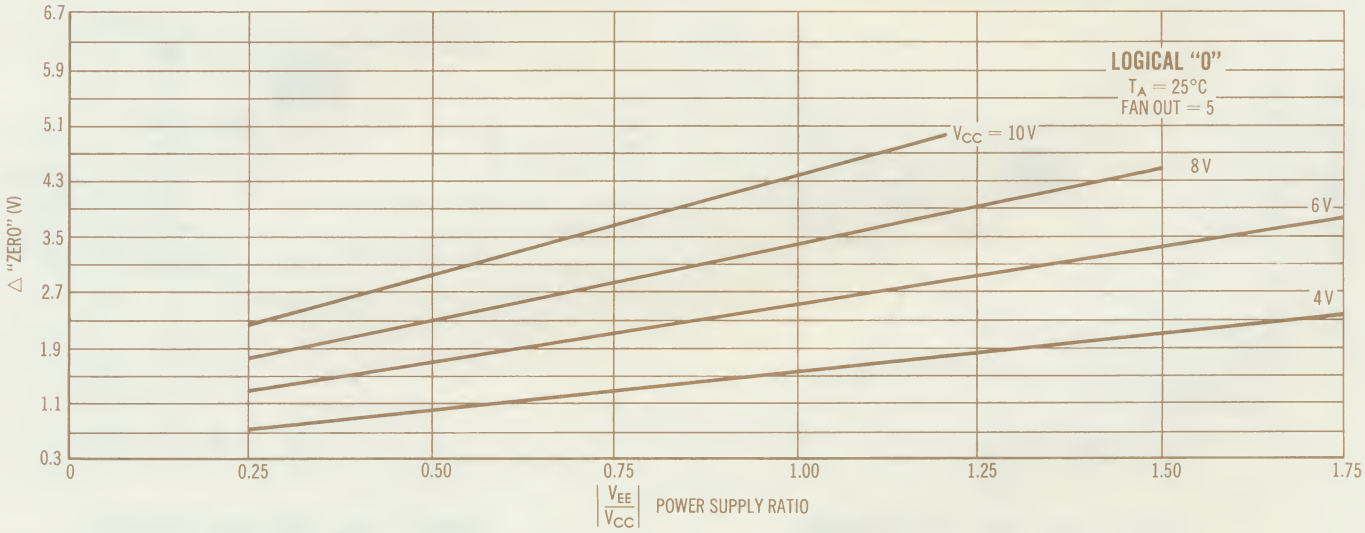
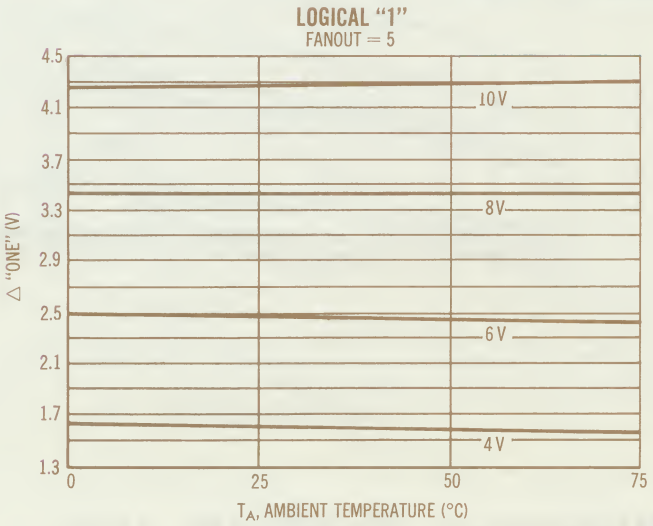


FIGURE 4 — INPUT DC NOISE MARGIN versus TEMPERATURE



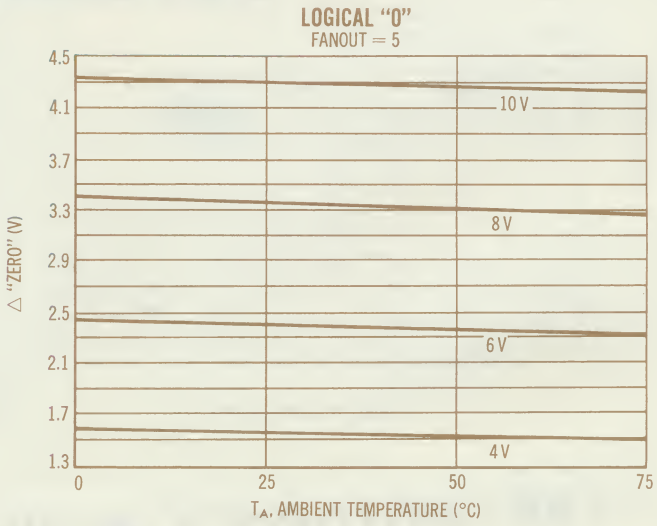


FIGURE 5 — GROUND NOISE IMMUNITY versus POWER SUPPLY RATIO

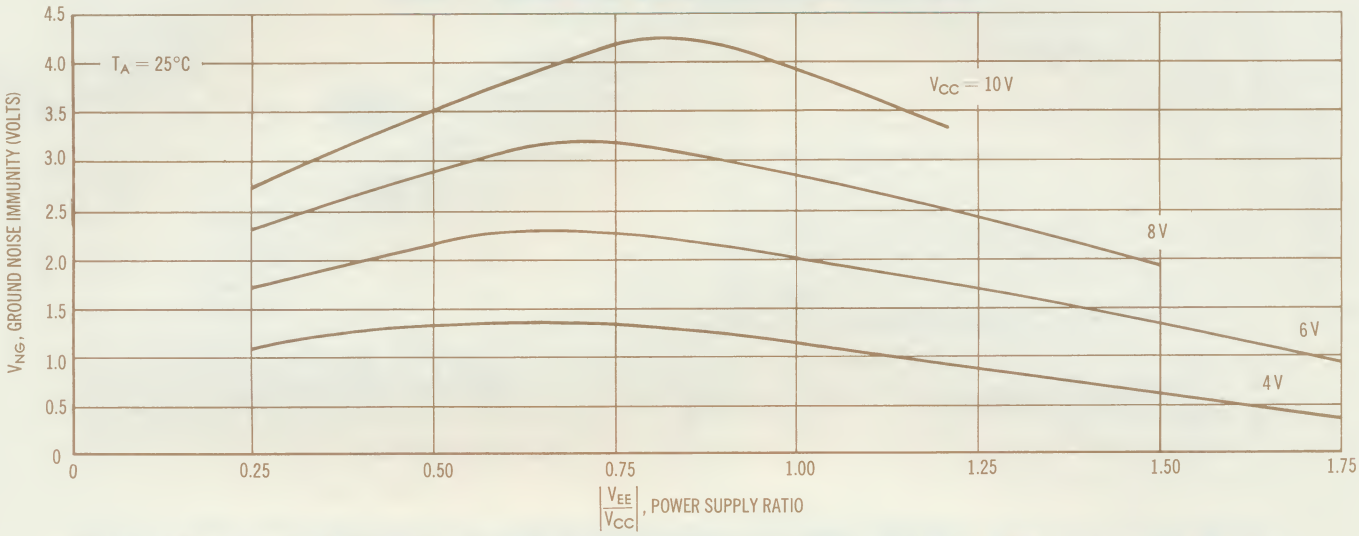


FIGURE 6 — POWER DISSIPATION versus POWER SUPPLY RATIO

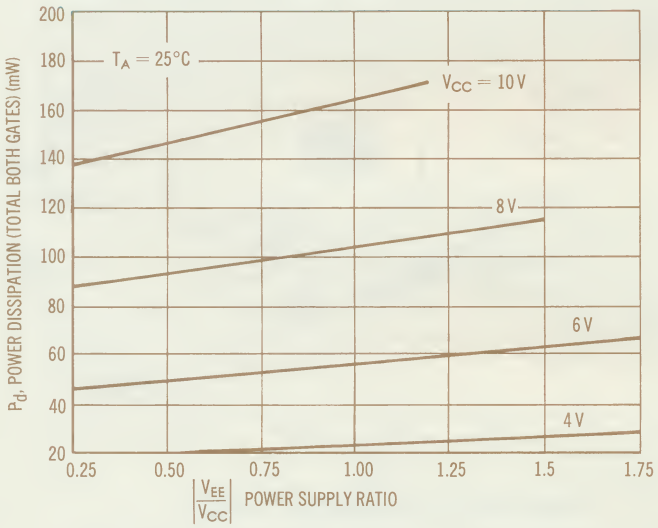
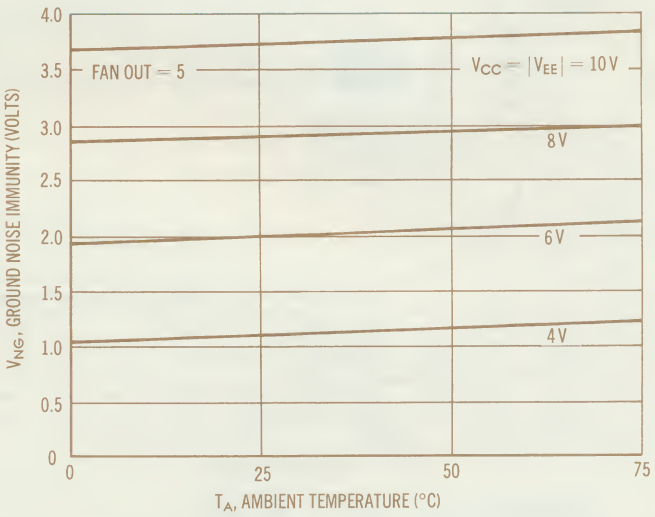


FIGURE 7 — GROUND NOISE IMMUNITY versus TEMPERATURE



TEST CIRCUITS

FIGURE 3 — INPUT NOISE MARGIN

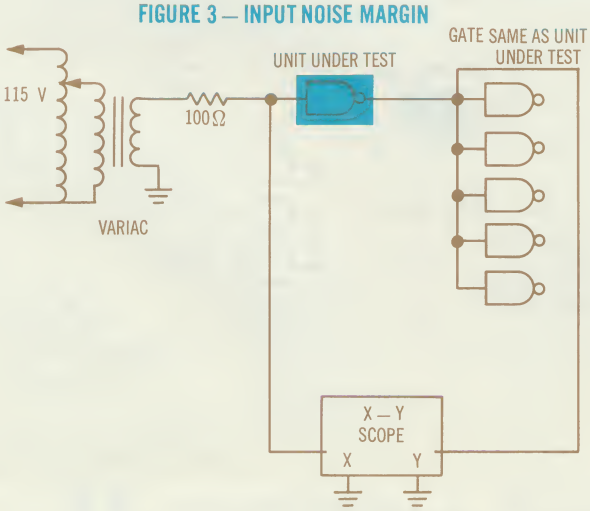
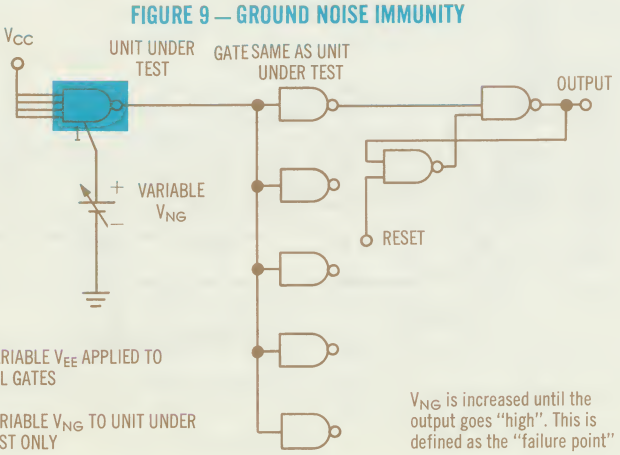


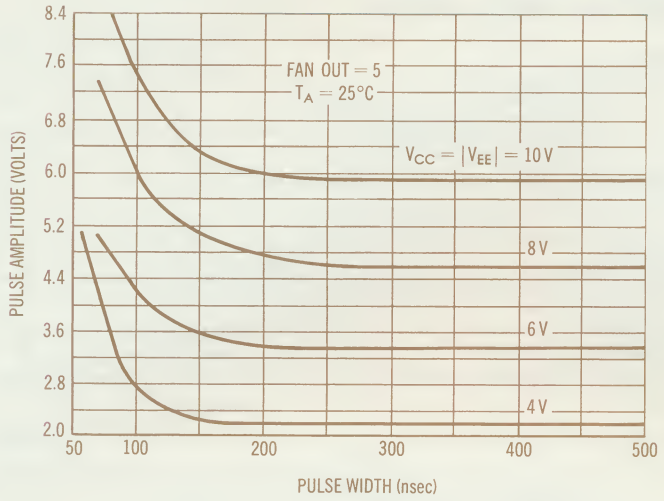
FIGURE 9 — GROUND NOISE IMMUNITY

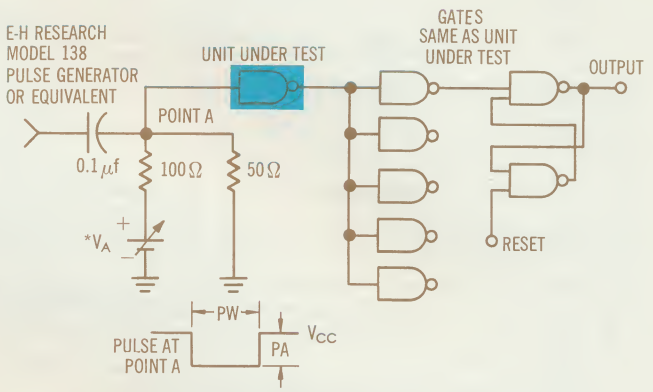


PULSE NOISE TESTS

For a given pulse width, the pulse amplitude is increased until the output goes "high". This is defined as the "Failure Point".

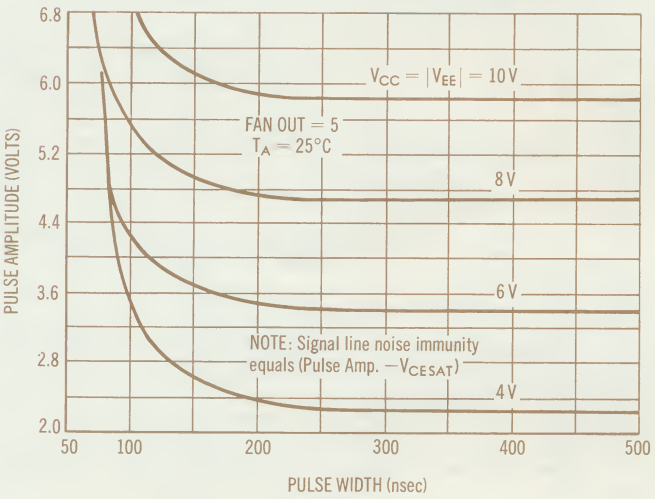
FIGURE 10 — SIGNAL-LINE NEGATIVE PULSE AMPLITUDE versus PULSE WIDTH





*Adjust for point A equal to V_{CC}

FIGURE 11 — SIGNAL-LINE POSITIVE PULSE AMPLITUDE versus PULSE WIDTH



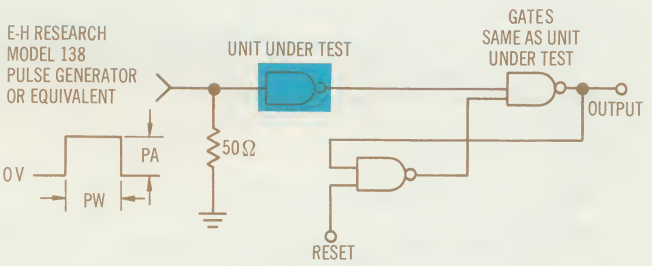
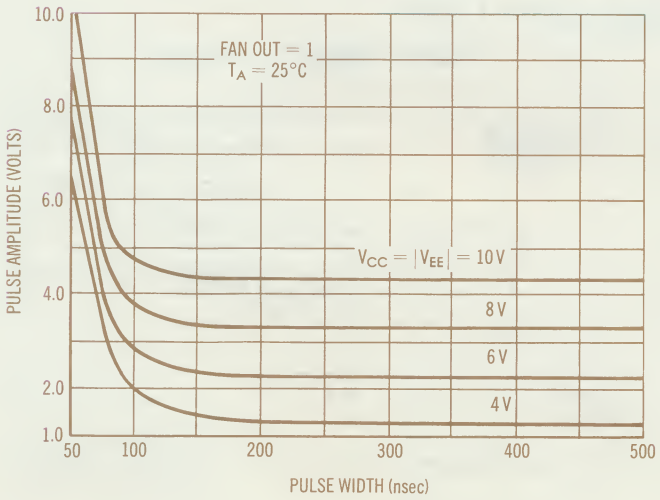


FIGURE 12 — GROUND-LINE POSITIVE PULSE AMPLITUDE versus PULSE WIDTH



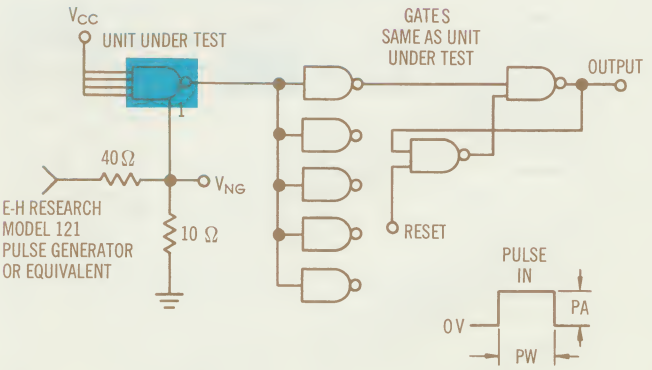


FIGURE 13 — t_{d2} PROPAGATION DELAY versus TEMPERATURE

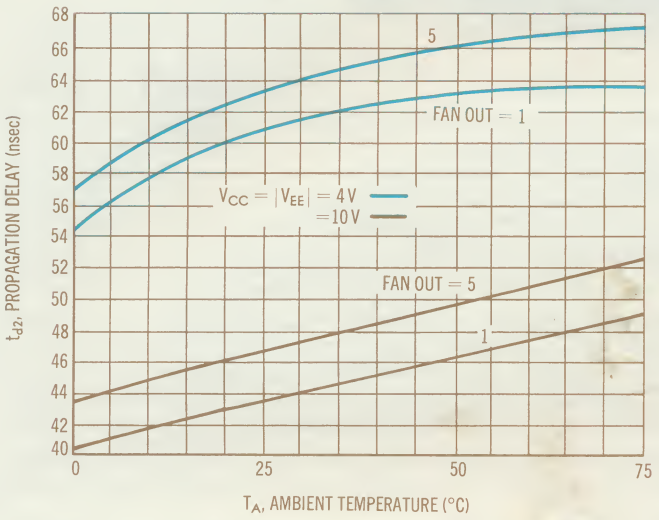


FIGURE 14 — t_{d1} PROPAGATION DELAY versus TEMPERATURE

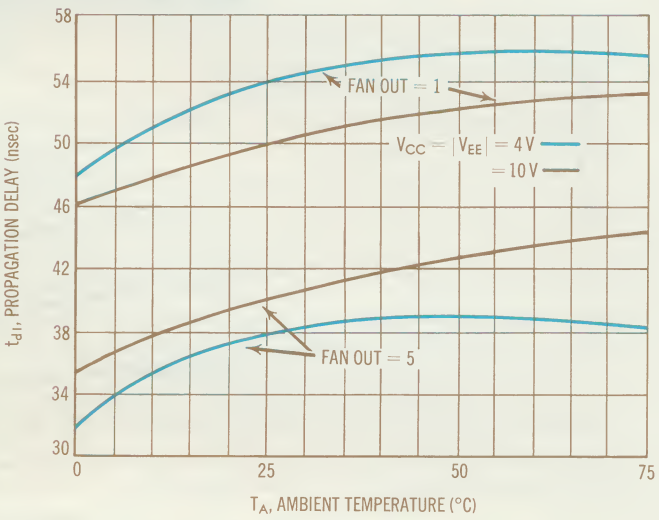


FIGURE 15 — AVERAGE PROPAGATION DELAY versus POWER SUPPLY RATIO

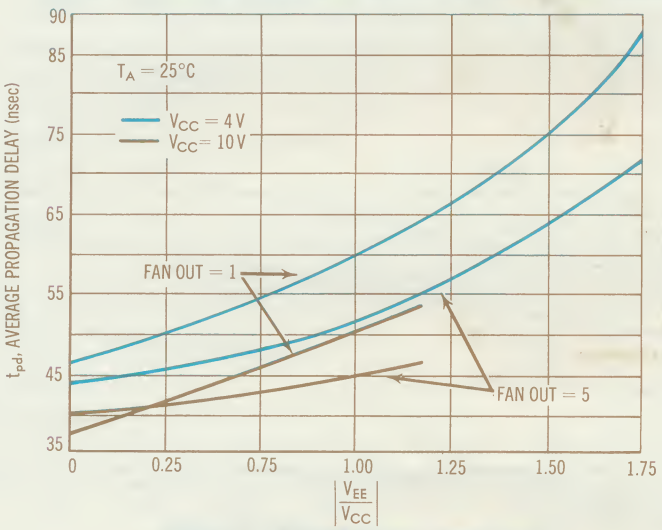
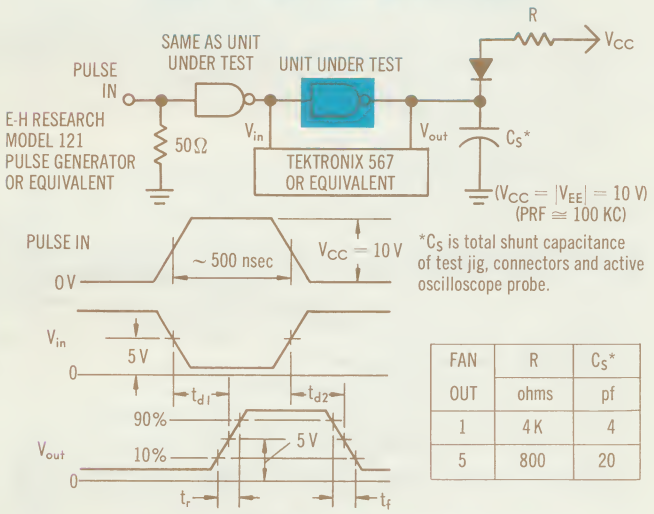


FIGURE 16 — SWITCHING TIME TEST CIRCUIT



*C_S is total shunt capacitance of test jig, connectors and active oscilloscope probe.

FAN OUT	R ohms	C_S* pf
1	4 K	4
5	800	20

FIGURE 17 — RISE TIME versus TEMPERATURE

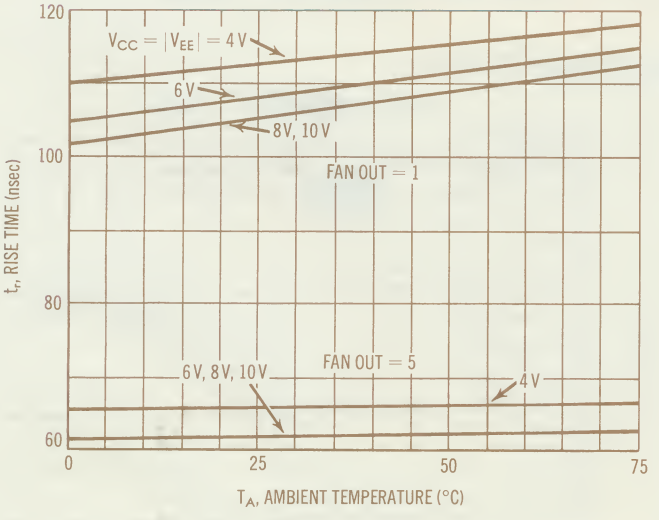
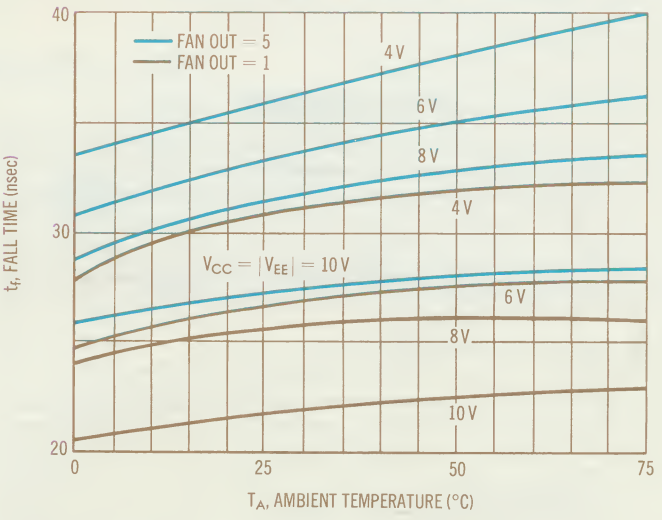


FIGURE 18 — FALL TIME versus TEMPERATURE



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